REMARKS

Claims 1-53 are pending. A clean copy of the claims with amendments incorporated is attached for the convenience of the Examiner.

In responding to the Examiner's prior art rejections, Applicant here only justifies the patentability of the non-allowed independent claims 1, 5, 11, 15, 22, 26, 30, 33, 37, 41, 46.[1] As the Examiner will appreciate, should these independent claims be patentable over the prior art, narrower dependent claims would also necessarily be patentable. Accordingly, Applicant does not separately discuss the patentability of the dependent claims, although it reserves the right to do so at a later time if necessary.

The Examiner has rejected all of the non-allowed independent claims 1, 5, 11, 15, 22, 26, 30, 33, 37, 41, 46 as anticipated by USP 6,747,997 ("Susnow"). In this rejection, the Examiner analogizes Susnow's PHY 681 (Fig. 6; col. 6, ll. 64-66) to Applicant's receiver; Susnow's decoders 740 (Fig. 7; abstract; col. 7, l. 63 – col. 8, l. 6) to Applicant's decoder; and Susnow's elastic buffer 682 (Figs. 6 & 7, col. 6, ll. 66-67; col. 8, ll. 32-36) to Applicant's output timing register.

As the Examiner will note, each of Applicant's rejected independent claims specify (using different language) the idea of receiving signals (e.g., at the receiver) in a first timing domain, decoding the signals (e.g., with a decoder), and outputting decoded signals (e.g., using an output timing register) in a second timing domain. Moreover, all non-allowed independent claims except claim 26 discussed further below (i.e., 1, 5, 11, 15, 22, 30, 33, 37, 41, 46) either originally specified or have been amended herein to specify (using various language) that that two timing domains are established in the various circuit blocks ***in accordance with separate clock signals***.

This is a significant difference, and mandates that Susnow cannot anticipate Applicant's claims.

As just noted, the Examiner suggests that the relevant aspects of Susnow's circuitry are the PHY 681, decoders 740, and elastic buffer 682. Starting first with Susnow's Figure 6, we see two timing domains, controlled by clocks RXCLK and CORE_CLK. PHY 681 is controlled in the first

---

1 Independent claim 50 has been allowed by the Examiner.

timing domain via clock signal RXCLK. However, the elastic buffer 682—which the Examiner's contends to correspond to Applicant's output timing register—is not shown in Figure 6 as receiving either the RXCLK or CORE_CLK clock signals, or any clock signal for that matter.

However, Figure 7, which provides a more detailed schematic of the PHY 681[1] and elastic buffer 682 portions of the circuit, provides additional clarity. Specifically, Figure 7 shows that ***all circuit blocks***, i.e., the PHY 681 (i.e., blocks 730, 740, and 750), the decoder 740, and the elastic buffer 682, ***receive the common PHY clock signal***.

In other words, all of the circuit blocks identified by the Examiner operate in accordance with a common clock signal. But this is not what Applicant claims in claims 1, 5, 11, 15, 22, 30, 33, 37, 41, 46. For example, claim 1, now amended, is quoted below. To help illustrate the error in the Examiner's rejection, the Examiner's purportedly analogous structures from Susnow are provided in brackets:

> 1. An apparatus for transferring signals between timing domains, comprising:
> a receiver ***[PHY 681?]*** for receiving a plurality of signals operative in a first timing domain ***in accordance with a first clock signal***;
> a decoder ***[decoder 740?]*** coupled to the receiver for at least partially decoding the signals to generate at least one decoded signal; and
> an output timing register ***[elastic buffer 682?]*** coupled to the decoder for outputting the at least one decoded signal in a second timing domain ***in accordance with a second clock signal.***

But as just noted, the elastic buffer 682 does not receive a different clock signal than that received by the PHY 681. Instead, the clock signal in Figure 7 is shown between these two circuit blocks to be the same. Therefore, this limitation is not met by Susnow.

In another example, original claim 11 recites.

> 11. An apparatus for transferring signals between timing domains, comprising:
> a receiver ***[PHY 681?]*** for capturing a plurality of signals ***timed to a capture clock***;
> a decoder ***[decoder 740?]*** coupled to the receiver for at least partially decoding the signals to generate at least one decoded signal; and
> an output timing register ***[elastic buffer 682?]*** coupled to the decoder ***for synchronizing the at least one decoded signal to a logic clock.***

Again, claim 11 calls for two distinct clocks signals, which Susnow does not disclosed with respect to the PHY 681 and the elastic buffer 682. The other claims are similar in this regard.

---

[1] As explained in the text of Susnow, the PHY 681 comprises the input registers 730, the decoders 740 and the link synchronization manager 750. See Col. 7, ll. 33-37.

Moreover, nothing in Susnow suggests the limitation of two distinct clocks, or suggests how his circuitry could even function were the elastic buffer 682 to receive a different clock (e.g., CORE_CLK of Fig. 6). Therefore, because Susnow does not disclose or suggest the separate clock signal limitations of claims 1, 5, 11, 15, 22, 30, 33, 37, 41, 46, Susnow cannot defeat the patentability of these claims for anticipation or for any other reason.

As for independent claim 26, that claim recites the receipt at the receiver of an "enable signal," and decoding or not at the decoder depending on the status of the enable signal. Susnow does not disclose this. Susnow is explicit about what his PHY block 681 and decoder 740 receives, and it does not include an enable signal. Instead, the received data includes only a eight-bit byte of data, a control bit, and an error bit:

> "The 2nd stage of PHY block 681 is the 8B/10B Decoders Unit 740. It is comprised of a pair of standard 8B/10B decoders connected in a cascaded configuration. Each decoder translates the 10-bit encoded data into an 8-bit data byte, a control bit and an associated error bit. The control bit specifies if the character is of data or control type. The error bit indicates the validity of the corresponding received data character. Thus the 20-bit raw data input is transformed into two 8-bit data bytes and 4 control signals for a total of 20 bits. These outputs are registered comprising the 2nd stage of the PHY block 681."

Susnow, col. 7, l. 63 to col. 8, l. 6.

Thus, Susnow does not disclose or suggest the limitation of "***a receiver*** for receiving a plurality of command signals operative in the sending clock domain ***and for receiving an enable signal with a first state in which the integrated circuit device is enabled and a second state in which the circuit device is not enabled***;"

* * * * *

The Applicant submits that pending claims 1-53 are patentable over the prior art of record, and requests that a Notice of Allowance issue for these claims.

Please feel free to contact the undersigned with any questions relating to this submission.

Respectfully submitted,

Terril G. Lewis
Registration No. 46,065

6-1-05
Date

Wong, Cabello, Lutsch, Rutherford
& Brucculeri, LLP
20333 SH 249
Houston, Texas 77070
(832) 446-2422
Fax: 832 446-2424

09/884,174

Convenience copy of claims with amendments incorporated

1. (Currently amended) An apparatus for transferring signals between timing domains, comprising:

    a receiver for receiving a plurality of signals operative in a first timing domain in accordance with a first clock signal;

    a decoder coupled to the receiver for at least partially decoding the signals to generate at least one decoded signal; and

    an output timing register coupled to the decoder for outputting the at least one decoded signal in a second timing domain in accordance with a second clock signal.

2. (Original) The apparatus of claim 1, wherein the plurality of signals include command signals and the at least one decoded signal includes at least one decoded command signal.

3. (Original) The apparatus of claim 1, wherein the plurality of signals include address signals and the at least one decoded signal includes at least one decoded address signal.

4. (Original) The apparatus of claim 1, wherein the first timing domain and the second timing domain have no predetermined phase relationship.

5. (Currently amended) An apparatus for transferring signals between timing domains, comprising:

    a receiver for receiving a plurality of signals operative in a first timing domain in accordance with a first clock signal, the receiver including a multiple-bit enabled register for each of the plurality of signals, each of the multiple-bit enabled registers being clocked using a first clock signal;

    a decoder coupled to the receiver for at least partially decoding the signals to generate at least one decoded signal; and

an output timing register coupled to the decoder for outputting the at least one decoded signal in a second timing domain in accordance with a second clock signal.

6. (Original) The apparatus of claim 5, wherein the receiver further includes a first ring counter for generating a multiple-bit enable signal, each of the bits of the enable signal being used for enabling clocking of one of the bits of the multiple-bit enabled registers.

7. (Original) The apparatus of claim 6, wherein the receiver further includes a multiplexer associated with each of the multiple-bit enabled registers for selecting one of the bits from the respective multiple-bit enabled register for output to the decoder.

8. (Original) The apparatus of claim 7, wherein the receiver further includes a second ring counter for generating a multiple-bit selection signal for each multiple-bit multiplexer.

9. (Original) The apparatus of claim 8, wherein the second ring counter selects a particular bit after the first ring counter selects the particular bit and before the first ring counter selects the particular bit again.

10. (Original) The apparatus of claim 5, wherein the output timing register is clocked using a second clock signal having no phase relationship with the first clock signal.

11. (Original) An apparatus for transferring signals between timing domains, comprising:

a receiver for capturing a plurality of signals timed to a capture clock;

a decoder coupled to the receiver for at least partially decoding the signals to generate at least one decoded signal; and

an output timing register coupled to the decoder for synchronizing the at least one decoded signal to a logic clock.

12. (Original) The apparatus of claim 11, wherein the plurality of signals include command signals and the at least one decoded signal includes at least one decoded command signal.

13. (Original) The apparatus of claim 11, wherein the plurality of signals include address signals and the at least one decoded signal includes at least one decoded address signal.

14. (Original) The apparatus of claim 11, wherein the capture clock and the logic clock have no predetermined phase relationship.

15. (Currently amended) An apparatus for transferring signals between timing domains, comprising:

a FIFO synchronizer having a front end and a back end, wherein the front end is for capturing a plurality of signals operative in a first timing domain in accordance with a first clock signal, and the back end is for synchronizing at least one decoded signal to a second timing domain in accordance with a second clock signal; and

a decoder coupled between the front and back ends of the FIFO synchronizer, the decoder for decoding the captured signals to generate the at least one decoded signal.

16. (Original) The apparatus of claim 15, wherein the plurality of signals include command signals and the at least one decoded signal includes at least one decoded command signal.

17. (Original) The apparatus of claim 15, wherein the plurality of signals include address signals and the at least one decoded signal includes at least one decoded address signal.

18. (Original) The apparatus of claim 15, wherein the front end of the FIFO synchronizer includes a multiple-bit enabled register for capturing each of the plurality of signals.

19. (Original) The apparatus of claim 18, wherein the front end of the FIFO synchronizer further includes a first ring counter for enabling each bit of the multiple-bit enabled register.

20. (Original) The apparatus of claim 19, wherein the front end of the FIFO synchronizer further includes a multiplexer associated with each multiple-bit enabled register for selecting one of the bits from the respective multiple-bit enabled register for output to the decoder.

21. (Original) The apparatus of claim 20, wherein the front end of the FIFO synchronizer further includes a second ring counter for generating a selection signal for each multiplexer.

22. (Currently amended) An integrated circuit device having a sending clock domain and a receiving clock domain, comprising:

a receiver for receiving a plurality of command signals operative in the sending clock domain in accordance with a sending clock signal;

a decoder coupled to the receiver for at least partially decoding the command signals to generate at least one decoded command signal; and

an output timing register coupled to the decoder for outputting the at least one decoded command signal in the receiving clock domain in accordance with a receiving clock signal.

23. (Original) The integrated circuit device of claim 22, further comprising a DRAM array.

24. (Original) The integrated circuit device of claim 23, wherein the plurality of command signals command a DRAM operation which is selected from the group of DRAM operations consisting of a read operation, a write operation and a refresh operation.

25. (Original) The integrated circuit device of claim 22, wherein the sending clock domain and the receiving clock domain have no predetermined phase relationship.

26. (Original) An integrated circuit device having a sending clock domain and a receiving clock domain, comprising:

a receiver for receiving a plurality of command signals operative in the sending clock domain and for receiving an enable signal with a first state in which the integrated circuit device is enabled and a second state in which the circuit device is not enabled;

a decoder coupled to the receiver for at least partially decoding the command signals to generate at least one decoded command signal if the circuit device is enabled; and

an output timing register coupled to the decoder for outputting the at least one decoded command signal in the receiving clock domain if the circuit device is enabled.

27. (Original) The integrated circuit device of claim 26, wherein the decoder inhibits decoding of the command signals if the circuit device is not enabled.

28. (Original) The integrated circuit device of claim 26, wherein the output of the at least one decoded command signal is inhibited if the circuit device is not enabled.

29. (Original) The integrated circuit device of claim 26, wherein the enable signal is a chip select signal.

30. (Currently amended) An apparatus for transferring signals between timing domains, comprising:

means for receiving a plurality of signals operative in a first timing domain in accordance with a first clock signal;

means for at least partially decoding the signals to generate at least one decoded signal; and

means for outputting the at least one decoded signal in a second timing domain in accordance with a second clock signal.

31. (Original) The apparatus of claim 30, wherein the plurality of signals include command signals and the at least one decoded signal includes at least one decoded command signal.

32. (Original) The apparatus of claim 30, wherein the plurality of signals include address signals and the at least one decoded signal includes at least one decoded address signal.

33. (Currently amended) A method of transferring signals between timing domains of a digital circuit, comprising:

receiving a plurality of signals operative in a first timing domain in accordance with a first clock signal;

at least partially decoding the signals to generate at least one decoded signal; and

outputting the at least one decoded signal in a second timing domain in accordance with a second clock signal.

34. (Original) The method of claim 33, wherein receiving the plurality of signals includes receiving command signals, and at least partially decoding the signals includes generating at least one decoded command signal.

35. (Original) The method of claim 33, wherein receiving the plurality of signals includes receiving address signals, and at least partially decoding the signals includes generating at least one decoded address signal.

36. (Original) The method of claim 33, wherein the first timing domain and the second timing domain have no predetermined phase relationship.

37. (Currently amended) A method of transferring signals between timing domains of a digital circuit, comprising:

capturing a plurality of signals in accordance with a capture clock of the digital circuit;

at least partially decoding the signals to generate at least one decoded signal; and

synchronizing the at least one decoded signal to a logic clock of the digital circuit.

38. (Original) The method of claim 37, wherein capturing the plurality of signals includes capturing command signals, and at least partially decoding the signals includes generating at least one decoded command signal.

39. (Original) The method of claim 37, wherein capturing the plurality of signals includes capturing address signals, and at least partially decoding the signals includes generating at least one decoded address signal.

40. (Original) The method of claim 37, wherein the capture clock and the logic clock have no predetermined phase relationship.

41. (Currently amended) A method of transferring signals between timing domains of a digital circuit using a first-in first-out (FIFO) synchronizer having a front end and a back end, comprising:

capturing a plurality of signals operative in a first timing domain at the front end of the FIFO synchronizer in accordance with a first clock signal;

transferring the signals from the front end of the FIFO synchronizer to a decoder;

decoding the signals at the decoder to generate at least one decoded signal;

transferring the at least one decoded signal to the back end of the FIFO synchronizer; and

synchronizing the at least one decoded signal to a second timing domain at the back end of the FIFO synchronizer in accordance with a second clock signal.

42. (Original) The method of claim 41, wherein capturing the signals includes capturing command signals, and decoding the signals includes generating at least one decoded command signal.

43. (Original) The method of claim 41, wherein capturing the signals includes capturing address signals, and decoding the signals includes generating at least one decoded address signal.

44. (Original) The method of claim 41, wherein capturing the signals includes clocking each signal into a multiple-bit enabled register using a first clock signal.

45. (Original) The method of claim 44, wherein synchronizing the at least one decoded signal includes inputting the at least decoded signal to an output timing register clocked using a second clock signal with no predetermined phase relationship with the first clock signal.

46. (Currently amended) A method of transferring command signals between a sending clock domain and a receiving clock domain of an integrated circuit device, comprising:

receiving a plurality of command signals operative in the sending clock domain of the integrated circuit device in accordance with a sending clock signal;

at least partially decoding the command signals to generate at least one decoded command signal; and

outputting the at least one decoded command signal in the receiving clock domain of the integrated circuit device in accordance with a receiving clock signal.

47. (Original) The method of claim 46, wherein the integrated circuit device includes a dynamic random access memory (DRAM).

48. (Original) The method of claim 47, wherein receiving the command signals includes receiving signals that command a DRAM operation selected from the group of DRAM operations consisting of a read operation, a write operation and a refresh operation.

49. (Original) The method of claim 46, wherein the sending clock domain and the receiving clock domain have no predetermined phase relationship.

50. (Original) A method of transferring command signals between a sending clock domain and a receiving clock domain of an integrated circuit device, comprising:

receiving a plurality of command signals operative in the sending clock domain of the integrated circuit device;

receiving an enable signal with a first state in which the integrated circuit device is enabled and a second state in which the integrated circuit device is not enabled; and

if the enable signal indicates that the integrated circuit device is enabled, decoding the command signals to generate at least one decoded command signal and outputting the at least one decoded command signal in the receiving clock domain of the circuit device.

51. (Original) The method of claim 50, further comprising, if the enable signal indicates that the integrated circuit device is not enabled, inhibiting decoding of the command signals.

52. (Original) The method of claim 50, further comprising, if the enable signal indicates that the integrated circuit device is not enabled, inhibiting outputting of the at least one decoded command signal.

53. (Original) The method of claim 50, wherein the enable signal is a chip select signal.